EE 330 Name_ _ _ _ _ _ _ _ _ _ _ _

Exam 2
Spring 2020 (March 13 2020)

Instructions: This is a 50-minute exam. Students may bring 2 pages of notes (front and back) to this exam. There are 10 short question is worth 2 points each and 5 problems worth 16 points each. Please solve problems in the space provided on this exam and attach extra sheets only if you run out of space in solving a specific problem.

If references to semiconductor processes are needed beyond what is given in a specific problem or question, assume all n-channel MOS transistors have model parameters $\mu_n C_{OX} = 350\mu A/V^2$ and $V_{Tn} = 0.5V$, all p-channel transistors have model parameters $\mu_p C_{OX} = 70\mu A/V^2$ and $V_{Tp} = -0.5V$. Correspondingly, assume all npn BJT transistors have model parameters $J_S = 10^{-14} A/\mu^2$ and $\beta=100$ and all pnp BJT transistors have model parameters $J_S = 10^{-14} A/\mu^2$ and $\beta = 25$. If the emitter area of a transistor is not given, assume it is $100\mu^2$. If parameters are needed for CMOS process characterization beyond what is given, use the measured parameters from the TSMC 0.18μ process given below as model parameters. Assume all diodes are characterized by the model parameters $J_{SX}=0.5A/\mu m^2$, $V_{G0}=1.17V$, and $m=2.3$.

1. (2 pts) What is the purpose of the n+ buried collector in a bipolar process?

2. (2 pts) What region of operation in a bipolar transistor corresponds to the saturation region of operation in a MOS transistor?

3. (2pts) Why is the β of the vertical npn transistor typically much larger than the β of the lateral pnp transistor in a typical bipolar process?

4. (2 pts) True or False: The carriers in the channel of a p-channel MOS transistor are minority carriers.

5 (2 pts) True or False: When operating in the forward active region the BE junction of a BJT is forward biased and the BC junction is reverse biased for both npn and pnp transistors?

6. (2pts) When biasing either MOS or Bipolar transistors, the Q-point is often placed near the middle of the load line. What is the major reason this is often done?

7. (2pts) The output characteristics of an npn transistor in the Forward Active region ideally show that the collector current is independent of V_{CE} but there is actually a small positive slope. What model parameter in the BJT is used to characterize this slope?

8. (2pts) When analyzing nonlinear circuits with a small-signal excitations, the nonlinear device models can always be used but often small-signal models are used instead. What is the major reason small-signal models are often used to analyze nonlinear circuits with small-signal excitations?

9. (2pts) If the same basic processing equipment is used, the area required for a minimum-sized vertical npn BJT is much larger than the area required for a minimum-sized n-channel MOSFET. What processing step in a bipolar process is the dominant contributor to the large area needed to form bipolar transistors?

10. (2pts) How many small-signal parameters are needed to characterize the small-signal operation of a nonlinear two-terminal circuit?

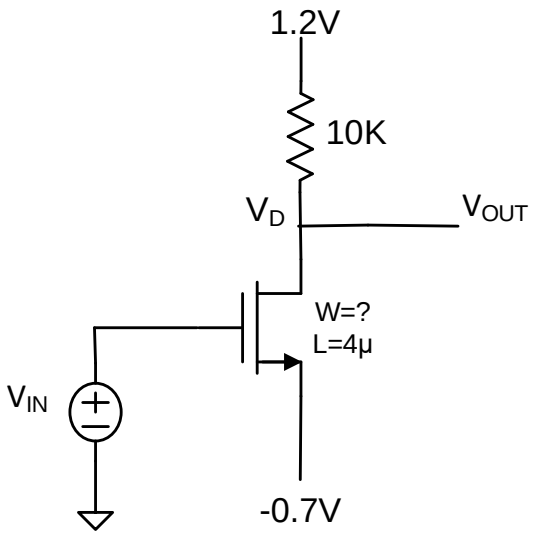
Problem 1 (16 pt) Consider the following circuit.

a) Draw the small signal equivalent circuit assuming the MOS transistor is operating in the saturation region

b) Give the small-signal voltage gain in terms of the small-signal model parameters assuming the MOS transistor is operating in the saturation region

c) Determine W so that the quiescent output voltage is 1V

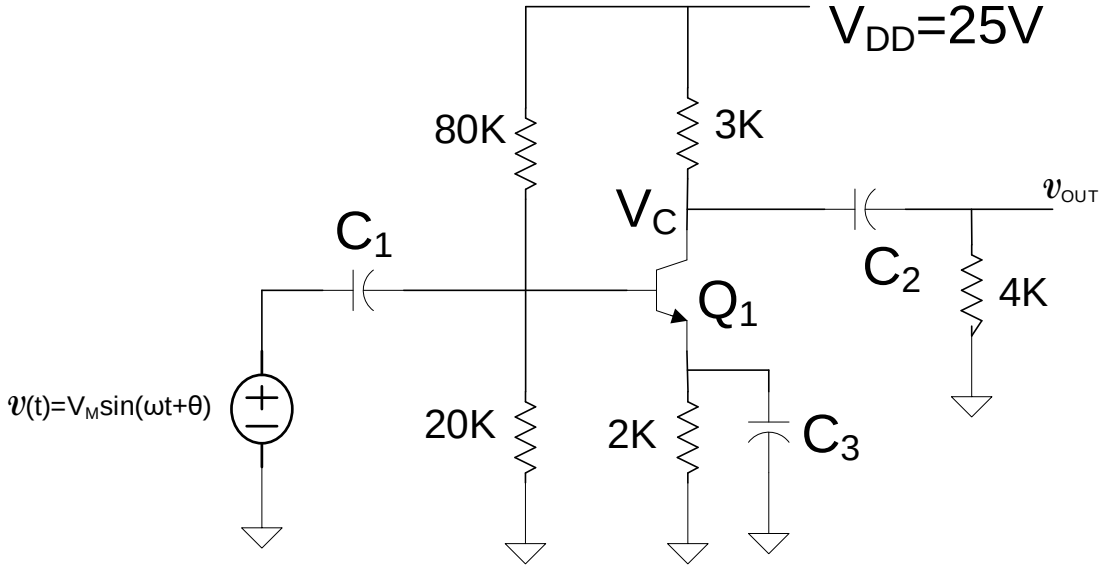
d) Determine the small-signal voltage gain with the value of W determined in part c)



Problem 2 Assume the capacitors are all very large.

a) Draw the small-signal equivalent circuit

b) Determine the quiescent value of V_C and V_{OUT}



Problem 3 The standard piecewise model of an n-channel MOSFET is given by the equations

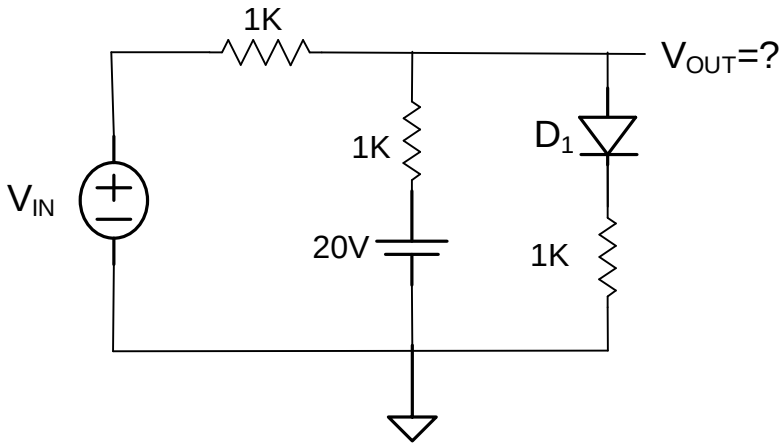
$$I_D=\begin{cases}0 & V_{GS}<V_{TH} \\ \dfrac{\mu C_{OX} W}{L}\left(V_{GS}-V_{TH}-\dfrac{V_{DS}}{2}\right)V_{DS} & V_{GS}>V_{TH},\quad V_{DS}<V_{GS}-V_{TH} \\ \dfrac{\mu C_{OX} W}{2L}\left(V_{GS}-V_{TH}\right)^2\left(1+\lambda V_{DS}\right) & V_{GS}>V_{TH},\quad V_{DS}>V_{GS}-V_{TH}\end{cases}$$

a) Determine the small-signal model of the n-channel MOSFET based upon this model when the device is operating in the triode region

b) Draw a small-signal equivalent circuit for the triode-region operation of the MOSFET

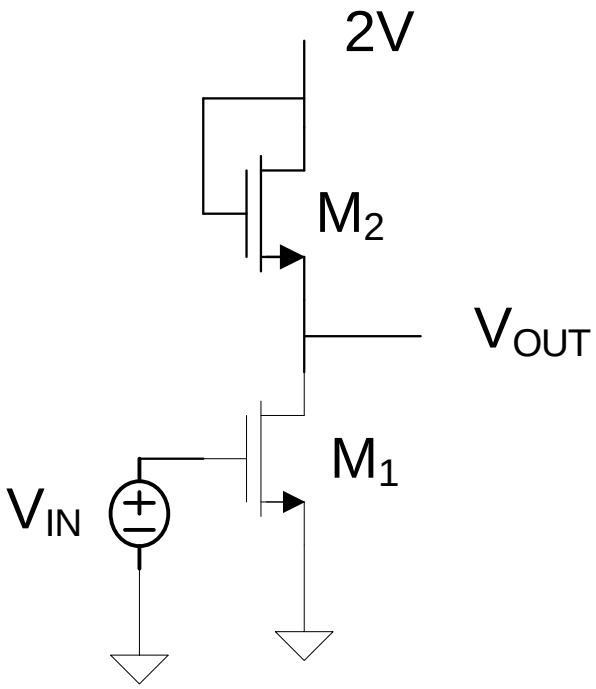
Problem 4 (16 pts) Consider the following circuit where the diode is assumed to be ideal.

a) Determine V_{OUT} if V_{IN} is a dc voltage source of value 25V.
b) Obtain an expression for V_{OUT} if $V_{IN}=50\sin(100t)$
c) Plot V_{OUT} for one period of the excitation if $V_{IN}=50\sin(100t)$



Problem 5 (16 pts) Consider the following circuit.

If V_{IN}=1V, determine the dimensions of M_1 that will result in an output voltage of 1V. Assume that the dimensions of M_2 are W_2=16μ and L_2=2μ. The relevant model parameters of the devices are V_{TN}=0.5V, V_{TP}=-0.5V, $\mu_n C_{OX}$=300μAV^{-2} and $\mu_p C_{OX}$=75μAV^{-2}.



MOSIS WAFER ACCEPTANCE TESTS

RUN: T68B (MM_NON-EPI) VENDOR: TSMC
TECHNOLOGY: SCN018 FEATURE SIZE: 0.18 microns
Run type: SKD

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: DSCN6M018_TSMC

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	0.27/0.18			
Vth		0.50	-0.51	volts
SHORT	20.0/0.18			
Idss		547	-250	uA/um
Vth		0.51	-0.51	volts
Vpt		4.8	-5.6	volts
WIDE	20.0/0.18			
Ids0		14.4	-4.7	pA/um
LARGE	50/50			
Vth		0.43	-0.42	volts
Vjbkd		3.1	-4.3	volts
Ijlk		<50.0	<50.0	pA
K' (Uo*Cox/2)		175.4	-35.6	uA/V^2
Low-field Mobility		416.52	84.54	cm^2/V*s

COMMENTS: Poly bias varies with design technology. To account for mask bias use the appropriate value for the parameters XL and XW in your SPICE model card.

Design Technology	XL (um)	XW um)
SCN6M_DEEP (lambda=0.09)	0.00	-0.01
thick oxide	0.00	-0.01
SCN6M_SUBM (lambda=0.10)	-0.02	0.00
thick oxide	-0.02	0.00

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>6.6	<-6.6	volts

PROCESS PARAMETERS	N+	P+	POLY	N+BLK	PLY+BLK	M1	M2	UNITS
Sheet Resistance	6.7	7.8	8.0	59.7	313.6	0.08	0.08	ohms/sq
Contact Resistance	10.6	11.0	10.0				4.79	ohms
Gate Oxide Thickness	41							angstrom

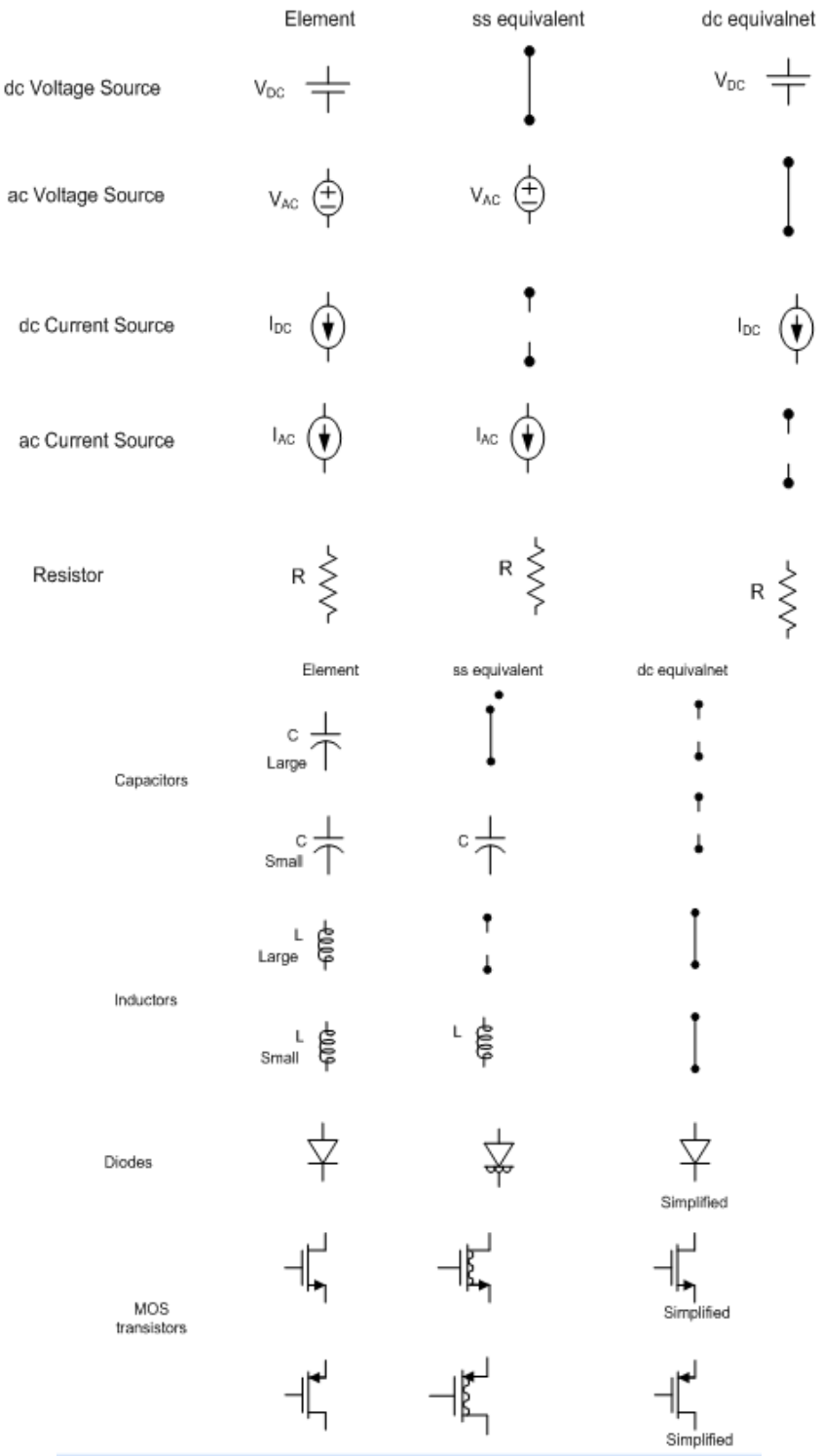
PROCESS PARAMETERS	M3	POLY_HRI	M4	M5	M6	N_W	UNITS
Sheet Resistance	0.08		0.08	0.08	0.03	930	ohms/sq
Contact Resistance	9.24		14.05	18.39	20.69		ohms

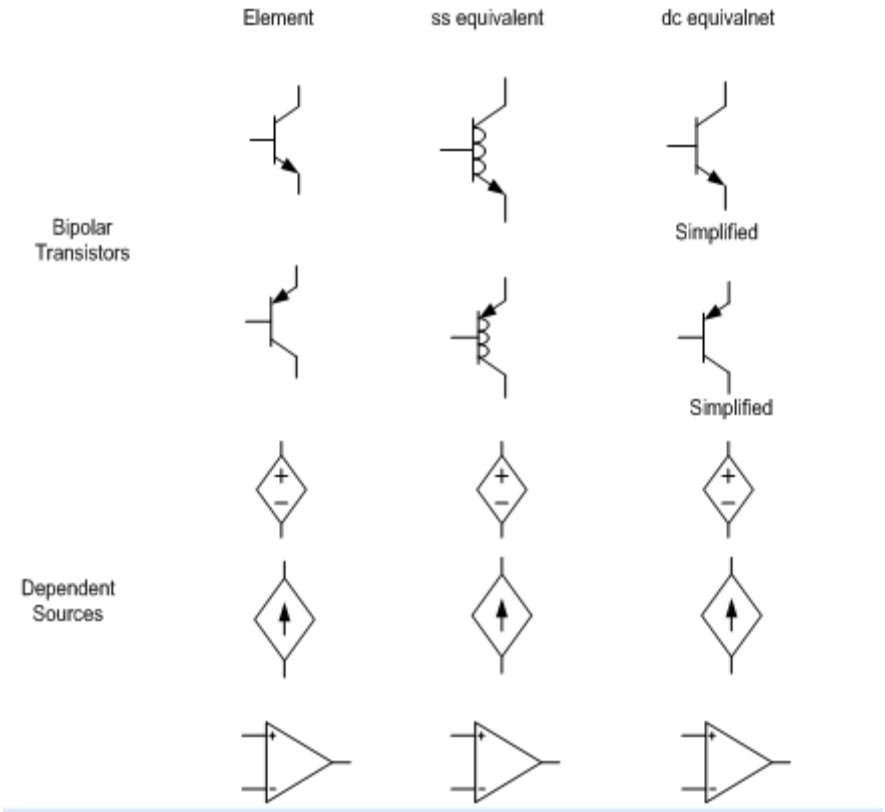
COMMENTS: BLK is silicide block.

CAPACITANCE PARAMETERS	N+	P+	POLY	M1	M2	M3	M4	M5	M6	R_W	D_N_W	M5P	N_W	UNITS
Area (substrate)	942	1163	106	34	14	9	6	5	3		123		125	aF/um^2
Area (N+active)			8484	55	20	13	11	9	8					aF/um^2
Area (P+active)			8232											aF/um^2
Area (poly)				66	17	10	7	5	4					aF/um^2
Area (metal1)					37	14	9	6	5					aF/um^2
Area (metal2)						35	14	9	6					aF/um^2
Area (metal3)							37	14	9					aF/um^2
Area (metal4)								36	14					aF/um^2
Area (metal5)									34				984	aF/um^2
Area (r well)	920													aF/um^2
Area (d well)										582				aF/um^2
Area (no well)	137													aF/um^2
Fringe (substrate)	212	235	41	35	29	21	14							aF/um
Fringe (poly)			70	39	29	23	20	17						aF/um
Fringe (metal1)				52	34		22	19						aF/um
Fringe (metal2)					48	35	27	22						aF/um
Fringe (metal3)						53	34	27						aF/um
Fringe (metal4)							58	35						aF/um
Fringe (metal5)								55						aF/um
Overlap (N+active)			895											aF/um
Overlap (P+active)			737											aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	0.74	volts
Vinv	1.5	0.78	volts
Vol (100 uA)	2.0	0.08	volts
Voh (100 uA)	2.0	1.63	volts
Vinv	2.0	0.82	volts
Gain	2.0	-23.72	
Ring Oscillator Freq.			
D1024_THK (31-stg,3.3V)		300.36	MHz
DIV1024 (31-stg,1.8V)		363.77	MHz
Ring Oscillator Power			
D1024_THK (31-stg,3.3V)		0.07	uW/MHz/gate
DIV1024 (31-stg,1.8V)		0.02	uW/MHz/gate

Dc and small-signal equivalent elements




Element
ss equivalent
dc equivalnet
Bipolar Transistors
Simplified
Simplified
Dependent Sources